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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/808,575 | 03/25/2004 | Kuniyuki Tani | 65933-081 | 5532 |

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| EXAMINER | |
|---|---|
| HERNANDEZ, WILLIAM | |
| ART UNIT | PAPER NUMBER |
| 2816 | |

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/808,575 | TANI ET AL. | |
| | Examiner | Art Unit | |
| | William Hernandez | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,11,18 and 20* is/are rejected.

7)☒ Claim(s) *6-8,10,12-17,19 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Applicant's amendment filed on 5/10/06 has been received and entered in the case. The amendment and argument presented therein overcome the informality objections, indefiniteness rejections and prior art rejections, and therefore, these are withdrawn. In view of the current reconsideration, new grounds of rejections are needed as set forth below. This action is NON-FINAL.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 9, 11, 18 and 20 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to teach how to make and use a control unit which switches the current driving capability of the driving unit according to a variation in the amount of current required by the load. Since there is no feedback shown in Fig. 3, it is unclear as to how the control unit switches the current driving capability of the driving unit according to a variation in the amount of current required by the load. This would

necessitate undue experimentation on the part of a person of ordinary skill in the art trying to make and use the invention.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 5, it is not understood how a transistor pair later becomes just a transistor in lines 8 and 10. It is suggested that "CMOS transistor" be changed to --CMOS transistor pair--.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Sim et al. (USP 6,456,555 B2).

Sim et al.'s Fig. 2 show a bias voltage generating circuit, comprising: a driving unit (100) which generates a bias voltage to be applied to a predetermined load (300); and

a control unit (controlling signal OMS) which switches a current driving capability of the driving unit according to a variation in an amount of current required for the load in a period for applying the bias voltage to the load (voltage generating circuits 110 and 120 are controlled by signal OMS depending on whether memory device is in normal mode or test mode; see col. 4: 53-57) as called for in claim 1.

Regarding claim 3, Sim et al.'s Fig. 2 shows the bias voltage generating circuit according to claim 1, wherein the driving unit includes a plurality of bias circuits (110 and 120) which are connected in parallel and have the same current driving capability (resistance values 112, 113, 122 and 123 can be controlled to achieve the same current driving capability; see col. 6: 61-65), and

the control unit (controlling signal OMS) switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits (via transistors 111, 114, 121 and 124).

7. Claims 1, 4 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Cusinato (USPAP 2004/0046684 A1).

Cusinato's Figs. 3-5 show a bias voltage generating circuit (42, Fig. 3), comprising: a driving unit (part of bias circuit 42) which generates a bias voltage ($I_{max}$ has a bias voltage associated with it) to be applied to a predetermined load (amplifier 46, Fig. 4); and

a control unit (phase generator 16, Fig. 3) which switches a current driving capability of the driving unit according to a variation in an amount of current required for the load in a period for applying the bias voltage to the load (amplifier 46 receives a variable current from bias circuit 42 depending upon a current phase generated by phase generator 16 which simultaneously controls the mode in which the amplifier operates; see page 2, paragraphs 25-30) as called for in claim 1.

Regarding claim 4, the recited limitations can clearly be seen in Cusinato's Figs. 3 and 4.

Regarding claim 11, Cusinato's Figs. 3-5 shows an amplifier circuit (44, Fig. 4), comprising:

an amplifier unit (46, Fig. 4) which repeats an auto-zero operation and an amplification operation alternately (amplifier unit 46 auto-zeroes during the sampling phase high and amplifies during the integration phase high; see Fig. 5 and pg. 2, paragraph 29);

a driving unit (42, Fig. 3) which supplies the amplifier unit with a bias voltage; and

a control unit (phase generator 16, Fig. 3) which switches the current driving capability of the driving unit according to a variation in an amount of current required between the auto-zero operation and the amplification operation of the amplifier unit (amplifier 46 receives a variable current from bias circuit 42 depending upon a current phase generated by phase generator 16 which simultaneously controls the mode in which the amplifier operates; see page 2, paragraphs 25-30).

8. Claims 1, 2 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Torrisi et al. (USP 6,784,721 B2).

Torrisi et al.'s Fig. 6 show a bias voltage generating circuit, comprising: a driving unit (10) which generates a bias voltage (Ig has a bias voltage associated with it) to be applied to a predetermined load (12); and

a control unit (sensing block 13 and comparator 14) which switches a current driving capability of the driving unit according to a variation in an amount of current required for the load in a period for applying the bias voltage to the load (comparator 14 controls switch SW which in turn controls the amount of current going into the output node) as called for in claim 1.

Regarding claim 2, Torrisi et al.'s Fig. 6 shows the bias voltage generating circuit according to claim 1, wherein the driving unit includes a plurality of bias circuits (GH and GL) which are connected in parallel and have different current driving capabilities (one sends $I_{high}$ and the other $I_{low}$ which corresponds to high current and low current, respectively), and

the control unit (13 and 14) switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits (via switch SW).

As per claim 9, this claim is rejected for the same reasons noted in claim 2.

***Allowable Subject Matter***

9. Claims 6-8, 10, 12-17, 19 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claim 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest a pipelined AD converter comprising an amplifier unit, a driving unit, and a control unit that switches the current driving power of the driving unit according to a variation in the amount of current required by the amplifier unit in combination with limitations "the control unit controls the current driving capability so as to drive the conversion unit at the initial stage with a relatively high current and drive the second and subsequent conversion units with a lower current" as called for in claim 21. Furthermore, the prior art of record also fails to teach the limitations of rejected claims 1, 2, 3 and 9 in combination with limitations of the bias circuits including a CMOS transistor pair composed of a PMOS transistor and an NMOS transistor connected in series between a power supply and ground and having a common drain connected to their respective gates along with two additional switches that control the operation of the bias circuits as called for in claims 5 and 6, and a bias circuit being a Wilson type current circuit with the recited configuration as called for in claim 10.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Matsuura (USP 6,198,337 B1), Fujihira (USP 5,159,516), Brkovic (USP 5,940,287) and Jacobs (USP 6,243,278 B1) are cited to teach driver circuits with a plurality of controllable bias circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WH

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TUAN T. LAM
PRIMARY EXAMINER